TECHNOLOGICAL IMPLEMENTATION PLAN

Description of project

EC PROGRAMME:	**IST**
PROJECT TITLE:	Architectures and Methodologies for Dynamic Reconfigurable Logic
ACRONYM:	**AMDREL**
PROGRAMME TYPE:	5th FWP (Fifth Framework Programme)
CONTRACT NUMBER:	IST-2001-34379
PROJECT WEB SITE (if any):	http://www.vlsi.ee.duth.gr/amdrel
START DATE:	01 Mar 2002
END DATE:	28 Feb 2005
COORDINATOR DETAILS:	**Name:** Konstantinos POTAMIANOS **Organisation:** INTRACOM S.A. **Address:** 19,5 Km Markopoulo Ave., 190 02 Peania, Greece **Telephone:** 210-6671486 **E-mail:** cpot@intracom.gr

PARTNERS NAME:
Democritus University of Thrace, Dimitrios SOUDRIS **Interuniversitair Micro-Electronica Centrum Vzw,** Serge VERNALDE **ST Microelectronics Belgium (STMB),** Alun FOSTER

Commission Officer Name:	Markus Korn

Executive summary

Original research objectives

The main objective of the proposed project is to develop methodologies, tools and intellectual property blocks to be integrated in a mixed granularity dynamically reconfigurable SOC implementation platform for the efficient realization of wireless communications systems. The proposed methodology, tools, reusable intellectual property blocks and the mixed granularity reconfigurable implementation platform will be used for the development of systems from the wireless telecom domain including critical parts of a wireless LAN system. Thus the project targets potential system design users from wireless telecom domain, where a good balance between "flexibility" and "implementation efficiency" is needed during product's life-time. More specificlly the ojectives of the project are: a) Development of systematic methodologies for high level design tasks (such as behavioural optimisation wrt different implementation related factors and especially wrt power consumption, partitioning of targeted functionality to different types of reconfigurable hardware); b) Development of reusable intellectual properties (including coarse granularity dynamically reconfigurable hardware blocks, low power fine-granularity configurable logic blocks); c) Instantiation of tools for implementation tasks; d) Establishment of a dynamically reconfigurable SOC platform with mixed granularity components (fine and coarse grain); e) Validation through demonstrators and; f) Dissemination and use of results.

Expected deliverables

D1 Behavioral optimization opportunities for wireless LAN systems, D2 Behavioral optimization requirements of reconfigurable platforms, D3 Requirements for interconnection networks in a dynamically reconfigurable context, D5 Refined mixed granularity dynamically reconfigurable target architecture template, D6 Selection of target implementation technology, D7 Existing functional level reconfigurable implementation platforms, D8 Critical functions from the target application domain suitable for implementation as reconfigurable blocks, D9 Survey of existing fine-grain reconfigurable hardware platforms, D10 Flexible and power efficient architectures

for functional dynamically reconfigurable hardware blocks, D11 Network building blocks, D12 Dissemination and Use Plan (DUP) including web site by DUTH, D14 Power efficient configurable logic block, D15 Interconnect network simulation model and interconnect network instance generator, D16 Quality Assurance Plan, D18 Behavioral optimization methodology for wireless LAN systems realized on reconfigurable platforms, D19 Strategy for functionality partitioning between mixed granularity reconfigurable hardware blocks, D20 Functional reconfigurable modules, D21 Prototype source-to-source behavioral optimizer, D22 Prototype partitioning software, D23 Optimized reusable soft intellectual properties for critical tasks of the target application domain, D24 Definition and realization of efficient control mechanism, D25 Systematic methodology for implementation on the functional reconfigurable hardware blocks, D26 Structure and organization of fine grain reconfigurable hardware, D27 Fine grain reconfigurable hardware generator, D25 Tool for technology mapping, D29 Placement and routing tools, D30 Configuration bitstream generator, D31 Validation of interconnect network (implementation and performance test), D32 High level executable models of selected demonstrators, D33 Updated Dissemination and Use Plan, D36 Demonstrator based on processor for critical parts of the baseband function of wireless LANsystem, D37 Demonstrator based on multimedia application processor for wireless terminals, D38 Evaluation of AMDREL approach, D39 Updated Dissemination and Use Plan, D40 Technology Implementation Plan (TIP).

Project's actual outcome

1) A mixed granularity dynamically reconfigurable SoC architecture template, 2) Systematic methodologies for behavioural optimisation and partitioning, 3) High level tools and reusable IPs, 4) Fine and coarse grain reconfigurable SoC components/interconnect network, 5) Real-life applications/demonstrators, 6) Dissemination to a wider community and use concluding activities.

Broad dissemination and use intentions for the expected outputs

Dissemination activities: a) Dissemination of the results through publications in workshops, seminars, conferences and magazines by all partners. b) Construction of a project web site, containing an overview of the project and to make available all public reports, and, journal and conference publications. c) Dissemination of the survey of fine-grain reconfigurable hardware, AMDREL methodology, design flows, and prototype tools through DUTH□s M.Sc. and Ph.D. programme. d) Seminars are organized by DUTH regularly every six months for the local university community (professors, undergraduate and graduate students), where members of VLSI Design and Testing Centre present their research results about the running projects. e) INTRACOM is considering Athens Information Technology (AIT) educational institute as another possible route for dissemination. Use plan: Use plan shall for the most part be through internalisation of the recommendations and associated methodology by the partners in their own product design flows. The commercial added value will appear as improved product development performance and market leadership in the chosen application field, which is a vital consideration for companies active in very fast-moving markets such as wireless networks. The academic partner and the research institute will largely exploit the project results through their inclusion into their portfolio of solutions. These are offered to their strategic partners via several contractual ways. This allows them to strengthen further their recognition as centers of excellence.

Overview of all your main project results

No.	Self-descriptive title of the result	Category A, B or C*	Partner(s) owning the result(s) (referring in particular to specific patents, copyrights, etc.) & involved in their further use
1	Network building blocks	B	Interuniversitair Micro-Electronica Centrum Vzw
2	Power efficient configurable logic block	B	Democritus University of Thrace
3	Interconnect network simulation model and interconnect network instance generator	B	Interuniversitair Micro-Electronica Centrum Vzw
4	Behavioural optimisation methodology and tool	B	INTRACOM S.A. Democritus University of Thrace
5	Optimised reusable soft intellectual properties for critical tasks of the target application domain	B	INTRACOM S.A. Democritus University of Thrace
6	Systematic methodology for implementation on the functional reconfigurable hardware blocks	B	ST Microelectronics Belgium (STMB)
7	Fine grain reconfigurable block and supporting tools	B	INTRACOM S.A. Democritus University of Thrace

*A: results usable outside the consortium / B: results usable within the consortium / C: non usable results

Quantified Data on the dissemination and use of the project results

Items about the dissemination and use of the project results (consolidated numbers)	Currently achieved quantity	Estimated future* quantity

Product innovations	0	0
Process innovations	2	2
New services (commercial)	0	0
New services (public)	1	1
New methods	1	1
Scientific breakthrought	1	1
Technical standards to which this project has contributed	0	0
EU regulations/directives to which this project has contributed	1	1
International regulations to which this project has contributed	0	0
PhDs generated by the project	2	5
Grantees/trainees including transnational exchange of personnel	276	300

** "Future" means expectations within the next 3 years following the end of the project*

Comment on European Interest

Community added value and contribution to EU policies

European dimension of the problem
Since future wireless communication products will require software and hardware reconfigurability to adapt to a variety of radio access bearers, evolving standards, variations of use and context requirements, it is evident that the existence of an integrated platform providing such features will help the European industry to maintain the leading position. Furthermore, the results of the project can be exploited by the European telecom industries as well as by various other SMEs/research institutes/design houses within Europe that deal with SoC designs for various applications in addition to telecom domain (e.g. automotive electronics, airplane/space electronics, etc.). Thus, the wide European community that will enjoy the benefits of the project results includes many different technological sectors; a very large group of engineers employed in all these sectors and of course the multi-millions of European citizens using the products of these industrial sectors.

Contribution to developing S&T co-operation at international level. European added value
Due to the nature of the project□s objectives it is not possible for a single company or research/academic institute to have the necessary expertise and deal alone with all tasks. Thus a European collaboration is needed for achieving successful results. AMDREL brings together a synergy of expertise that exists in various industrial and research/academic sites in Europe. Specifically the project involves expertise of the following partners: a) a system company, with experience and technological background in telecommunications and strong interest in incorporating reconfigurable technology in future products, b) an IC manufacturer and design company dealing with IC design/fabrication and development of telecom products also interested in incorporating reconfigurable technology in future products, c) institute/university partners with experience in design methodology development, prototype design support tools, low-power VLSI design.

Contribution to policy design or implementation
It is self-evident that the innovations introduced by the AMDREL project,contribute to the Innovation Policy, while the project contributes to the Employment and Social Policy. In addition, the Technology Policy, which promotes the convergence of telecommunications, media and information technologies, is contributed by AMDREL since the workprogramme objectives are properly addressed. Finally, via dissemination actions of the project, SMEs will benefit in acquiring valuable SoC design methodology/tool knowledge to them, which would be extremely difficult to obtain on their own, thus contributing to EU□s SME Policy. Furthermore, the presence of partners from different EC countries in the consortium: □Advances the communication and cooperation between design/research groups coming from different EC members□.

Contribution to Community social objectives

Improving the quality of life in the Community:
Project□s contribution to the improvement of quality of life mainly concerns the use of products to be developed based on AMDREL□s results. Specifically mobile phones as well as broadband wireless communication systems (which are the basic target applications of reconfigurable SoCs) play a key role in various fields of every day life such as: Office automation, Financial services, Medical and hospital systems, Education and training and Ad-hoc networking.

Provision of appropriate incentives for monitoring and creating jobs in the Community (including use and development of skills):
The contribution to the improvement of employment is direct and indirect. The direct contribution by the project relates to the new job positions that will be created for SoC design engineers, telecommunication engineers and marketing staff (technology-employed citizens). The indirect contribution, which is more significant, relates to the variety of applications and services described above that will be supported, thus opening new opportunities for employment that will mostly require skilled personnel.

Supporting sustainable development, preserving and/or enhancing the environment (including

use/conservation of resources):
N/A

Expected project impact (to be filled in by the project coordinator)

EU Policy Goals	I SCALE OF EXPECTED IMPACT OVER THE NEXT 10 YEARS -1 0 1 2 3	II other	
		Not applicable to project	Project Impacttoo difficult to estimate
1. Improved sustainable economic development and growth, competitiveness	2		
2. Improved employment	2		
3. Improved quality of life and health and safety	0	√	
4. Improved education	3		
5. Improved preservation and enhancement of the environment	0	√	
6. Improved scientific and technological quality	3		
7. Regulatory and legislative environment	0	√	
8. Other	0	√	

1. Economic development and growth, competitiveness	Scale of Expected Impacts over the next 10 years (2)	
	By Project End -1 0 1 2 3	After Project End -1 0 1 2 3
a) Increased Turnover for project participants - national markets	2	2
b) Increased Turnover for project participants - international markets	2	2
c) Increased Productivity for project participants	2	2
d) Reduced costs for project participants	2	2
e) Improved output quality/high technology content	2	2

2. Employment	Scale of Expected Impacts over the next 10 years (2)	
	By Project End -1 0 1 2 3	After Project End -1 0 1 2 3
a) Safeguarding of jobs	2	2
b) Net employment growth in projects participants staff	2	2
c) Net employment growth in customer and supply chains	2	2
d) Net employment growth in the European economy at large	2	2

3. Quality of Life and health and safety	Scale of Expected Impacts over the next 10 years (2)	
	By Project End -1 0 1 2 3	After Project End -1 0 1 2 3
a) Improved health care		
b) Improved food, nutrition		
c) Improved safety (incl. consumers and workers safety)		

d) Improved quality of life for the elderly and disabled	
e) Improved life expectancy	
f) Improved working conditions	
g) Improved child care	
h) Improved mobility of persons	

4. Improved education	**Scale of Expected Impacts over the next 10 years (2)** **By Project End** -1 0 1 2 3	**After Project End** -1 0 1 2 3
a) Improved learning processes including lifelong learning	3	2
b) Development of new university curricula	3	2

5. Preservation and enhancement of the environment	**Scale of Expected Impacts over the next 10 years (2)** **By Project End** -1 0 1 2 3	**After Project End** -1 0 1 2 3
a) Improved prevention of emissions		
b) Improved treatment of emissions		
c) Improved preservation of natural resources and cultural heritage		
d) Reduced energy consumption		

6. S&T quality	**Scale of Expected Impacts over the next 10 years (2)** **By Project End** -1 0 1 2 3	**After Project End** -1 0 1 2 3
a) Production of new knowledge	3	2
b) Safeguarding or development of expertise in a research area	3	2
c) Acceleration of RTD, transfer or uptake	3	2
d) Enhance skills of RTD staff	3	2
e) Transfer expertise/know-how/technology	3	2
f) Improved access to knowledge-based networks	2	1
g) Identifying appropriate partners and expertise	1	1
h) Develop international S&T co-operation	1	1
i) Increased gender equality	0	0

7. Regulatory and legislative environment	**Scale of Expected Impacts over the next 10 years (2)** **By Project End** -1 0 1 2 3	**After Project End** -1 0 1 2 3
a) Contribution to EU policy formulation		
Contribution to EU policy implementation		

8. Other (please specify)	**Scale of Expected Impacts over the next 10 years (2)** **By Project End** -1 0 1 2 3	**After Project End** -1 0 1 2 3

Description of Results

No.	Title
1	Network building blocks

CONTACT PERSON FOR THIS RESULT

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Specific Result URL	

SUMMARY

This result is an IP library of VHDL building blocks that can be used to build interconnect networks with different topologies on reconfigurable architectures. Such networks enable the dynamic creation and deletion of tasks on the reconfigurable hardware through their unified application interface. They form the basic components to explore and implement different interconnect networks depending on the requirements of the applications.

SUBJECT DESCRIPTORS CODES

120 COMMUNICATION ENGINEERING/TECHNOLOGY
129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL
155 DESIGN, DESIGN ENGINEERING
336 INTELLECTUAL PROPERTY
395 MICROELECTRONICS
599 SYSTEMS DESIGN/THEORY
600 SYSTEMS ENGINEERING

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential
Deliverable D11	Network building blocks	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details (reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for	√					√	EP 1372084 / US 2004-0049672
Patent granted							
Patent search carried out							
Registered design							

Trademark applications						
Copyrights						
Secret know-how						
Other - please specify:						

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
30 Manufacture of office machinery and computers 32 Manufacture of radio, television and communication ☐ 72 Computer and related activities 73 Research and development

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	**Actual current quantity**	**Estimated (or future) quantity**
Time to application / market (in months from the end of the research project)	0	0
Number of (public or private) entities potentially involved in the implementation of the result:	1	2
of which: number of SMEs:	0	0
of which: number of entities in third countries (outside EU):	1	2
Targeted user audience: of reachable people	5	5
S&T publications (referenced publications only)	7	3
publications addressing general public (e.g. CD-ROMs, WEB sites)	1	1
publications addressing decision takers / public authorities / etc.	1	0
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement	√	**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
2	Power efficient configurable logic block

CONTACT PERSON FOR THIS RESULT

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URL	www.duth.gr
Specific Result URL	http://vlsi.ee.duth.gr/~dsoudris

SUMMARY

The result is the detailed architecture design of a power efficient configurable logic block (CLB), taking into consideration the constraints and limitations of the design supporting tools. Full-custom design using the chosen silicon technology of 0.18 um STM technology, exhaustive design exploration for selecting optimal design parameters, for instance number of look-up table inputs, in terms of power, area, and performance provided the appropriate results regarding with the design of configurable block. The low-energy CLB design of was the first critical step for implementing efficient low-energy fine-grain reconfigurable hardware.

SUBJECT DESCRIPTORS CODES
155 DESIGN, DESIGN ENGINEERING 129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL 336 INTELLECTUAL PROPERTY 395 MICROELECTRONICS 599 SYSTEMS DESIGN/THEORY

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential
Deliverable D14	Power efficient configurable logic block	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details (reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights	√			journal and conference publications			
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
30 Manufacture of office machinery and computers 32 Manufacture of radio, television and communication ☐ 72 Computer and related activities 73 Research and development 80 Education

CURRENT STAGE OF DEVELOPMENT

Current stage of development	Experimental development stage (laboratory prototype)
Other:	

Quantified data about the result

Items (about the results)	**Actual current quantity**	**Estimated (or future) quantity**
Time to application / market (in months from the end of the research project)	12	24
Number of (public or private) entities potentially involved in the implementation of the result:	1	2
of which: number of SMEs:	1	1
of which: number of entities in third countries (outside EU):	0	1
Targeted user audience: of reachable people	4	9
S&T publications (referenced publications only)	7	2
publications addressing general public (e.g. CD-ROMs, WEB sites)	1	1
publications addressing decision takers / public authorities / etc.	0	0
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	√
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
3	Interconnect network simulation model and interconnect network instance generator

CONTACT PERSON FOR THIS RESULT

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URL	http://www.imec.be/
Specific Result URL	

SUMMARY

This result provides the usage support to allow designers to build and integrate an interconnect network in several applications, using a library of network building blocks (D11). It consists of two major components. The first component comprises the simulation models of the network, which enables the modeling of the complete system that runs on the reconfigurable platforms. It allows to see the impact of different network technologies. The second component consists of the network instance generators, which will allow the designer to create a network according to the structure of the reconfigurable system he/she wants to develop.

SUBJECT DESCRIPTORS CODES
120 COMMUNICATION ENGINEERING/TECHNOLOGY 129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL 155 DESIGN, DESIGN ENGINEERING 395 MICROELECTRONICS 599 SYSTEMS DESIGN/THEORY 600 SYSTEMS ENGINEERING

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential
Deliverable D15	Interconnect network simulation model and interconnect network instance generator	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details (reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for	√					√	EP 1372084 / US 2004-0049672
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights							
Secret know-how							
Other - please							

specify:						

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
30 Manufacture of office machinery and computers 32 Manufacture of radio, television and communication ☐ 72 Computer and related activities 73 Research and development

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	**Actual current quantity**	**Estimated (or future) quantity**
Time to application / market (in months from the end of the research project)	0	0
Number of (public or private) entities potentially involved in the implementation of the result:	1	2
of which: number of SMEs:	0	0
of which: number of entities in third countries (outside EU):	1	2
Targeted user audience: of reachable people	5	5
S&T publications (referenced publications only)	7	3
publications addressing general public (e.g. CD-ROMs, WEB sites)	1	1
publications addressing decision takers / public authorities / etc.	1	0
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement	√	**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
4	Behavioural optimisation methodology and tool

CONTACT PERSON FOR THIS RESULT

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E-mail	dsoudris@ee.duth.gr
URL	www.duth.gr
Specific Result URL	http://vlsi.ee.duth.gr/amdrel

SUMMARY

The results are: i) the development of a systematic design methodology towards behavioral-level optimisation,and especially, the development of a novel methodology for energy- and performance-optimized design of dynamic memory allocators and ii) the development of a prototype design support software for addressing time-consuming task of dynamic memory management of the behavioral optimization approach. More specifically, the methodology is already finalized and the corresponding tool was completed by end of June 2004. Both methodology and tools target to wireless telecom applications.

SUBJECT DESCRIPTORS CODES
120 COMMUNICATION ENGINEERING/TECHNOLOGY 129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL 155 DESIGN, DESIGN ENGINEERING 395 MICROELECTRONICS 399 MOBILE COMMUNICATIONS 599 SYSTEMS DESIGN/THEORY 600 SYSTEMS ENGINEERING 609 TELECOMMUNICATION ENGINEERING/TECHNOLOGY

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential
Deliverable D18	"Behavioral optimisation methodology for wireless LANnsystems realized in reconfigurable platforms" The deliverable D18 adresses a systematic methodology for the implementation oriented behavioral optimization of high level descriptions of target systems. The implementation factors, on which the methodology focus, include data storage and transfers, namely dynamic data type refinement and dynamic memory management. The methodology consists of: a) the dynamic data type (DDT) refinement and b) the dynamic memory management (DMM) refinement.	Confidential
Deliverable D21	"Prototype source-to-source behavioral optimizer" The deliverable D21 addresses the development of prototype source-to-source tool for the automation of the behavioral optimizations methodology. The main automation provided by our tool consist of the creation of highly customized dynamic memory managers with the use of DM Libraries that are part of the tool. The other automation consists of a tool to automate the transformation of C object oriented source code to procedural source code.	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details	Pre-existing know-how Tick a box and give the

	(reference numbers, etc) if appropriate					corresponding details (reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights	√			journal and conference publications			
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
30 Manufacture of office machinery and computers 32 Manufacture of radio, television and communication ☐ 72 Computer and related activities 73 Research and development

CURRENT STAGE OF DEVELOPMENT

Current stage of development	Software code
Other:	

Quantified data about the result

Items (about the results)	Actual current quantity	Estimated (or future) quantity
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	√
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	√

Other	(please specify)		
Details:			

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
5	Optimised reusable soft intellectual properties for critical tasks of the target application domain

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Organisation	Democritus University of Thrace
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Telephone	25410-79557
Fax	25410-79545
E-mail	dsoudris@ee.duth.gr
URL	www.duth.gr
Specific Result URL	http://vlsi.ee.duth.gr/amdrel

SUMMARY

The result is an IP library of reusable VHDL-described components, which can perform critical tasks of systems in the targeted wireless communications domain. The main focus is on IPs for FFT, FIR filtering, taking into consideration plethora of design parameters will be delivered. These descriptions can be either directly mapped on the available reconfigurable hardware or used as input for the development of optimised lower level descriptions that can be directly on the available reconfigurable hardware.

SUBJECT DESCRIPTORS CODES
129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL 155 DESIGN, DESIGN ENGINEERING 336 INTELLECTUAL PROPERTY 395 MICROELECTRONICS 599 SYSTEMS DESIGN/THEORY 120 COMMUNICATION ENGINEERING/TECHNOLOGY

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential
Deliverable D23	Optimized reusable soft intellectual properties for critical tasks of the target application domain	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details (reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights	√			journal and conference publications			
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
30 Manufacture of office machinery and computers 32 Manufacture of radio, television and communication ☐ 72 Computer and related activities 73 Research and development 80 Education

CURRENT STAGE OF DEVELOPMENT

Current stage of development	Software code
Other:	

Quantified data about the result

Items (about the results)	**Actual current quantity**	**Estimated (or future) quantity**
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement	√	**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	√
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
6	Systematic methodology for implementation on the functional reconfigurable hardware blocks

CONTACT PERSON FOR THIS RESULT

Name	Alun FOSTER
Position	External projects manager
Organisation	ST Microelectronics Belgium (STMB)
Address	Excelsiorlaan 44-46 1390, Zaventem Belgium
Telephone	
Fax	
E-mail	alun.foster@st.com
URL	
Specific Result URL	

SUMMARY

The methodology for implementing coarse-grained reconfigurable blocks begins from a high-level descritpion in SystemC. From the timed-functional description, a bridge is required to the implementation level. The methodology describes how to use an off-the-shelf design tool (from Target Compiler Technologies) to take timed functional models from SystemC and use a dedicated VLIW architecture as a physical instantiation of a coarse-grained reconfigurable block. Reconfiguration is achieved by providing the block with context-dependent machine code, controlled via externally applied switch options (the methodology also describes various methods for implementing this). The hardware definition of the reconfigurable engine is derived from an intermediate abstraction language "nML" which produces a dedicated compiler (C to machine code), a synthesisable HDL descritpion, and an instruction set simulator used to model the block at the cycle-accurate level in SystemC. The methodology permits iteration on the block architecture to be carried out very quickly, with immediate feedback on system performance through the integration into the complete SystemC environment. The use of a VLIW implementation does penalise memory requirements (programme store). However, this methodology is estimated to reduce the design time complex functions in multi-processor chains by as much as 50% compared to the "manual" methods presently available. The methodology is particularly applicable to, but not limited to, pipe-lined or daisy-chained computational tasks that must be implemented in an embedded sytem or integrated circuit.

SUBJECT DESCRIPTORS CODES
192 ELECTRONICS, ELECTRONIC ENGINEERING 155 DESIGN, DESIGN ENGINEERING 204 ENGINEERING, CONCURRENT ENGINEERING 395 MICROELECTRONICS

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential
IST-2001-34379-WP3-D24	Definition and Realization of an Efficient Control Mechanism	Confidential
IST-2001-34379-WP3-D25	Systematic Methodology for implementation of (coarse-grained) Reconfigurable Hardware Blocks	Public

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details (reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							

Patent search carried out						
Registered design						
Trademark applications						
Copyrights						
Secret know-how						
Other - please specify:						

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
32 Manufacture of radio, television and communication ☐ 72 Computer and related activities 73 Research and development

CURRENT STAGE OF DEVELOPMENT

Current stage of development	Guidelines, methodologies, technical drawings
Other:	Mthodology for internal use

Quantified data about the result

Items (about the results)	**Actual current quantity**	**Estimated (or future) quantity**
Time to application / market (in months from the end of the research project)	12	3
Number of (public or private) entities potentially involved in the implementation of the result:	0	1
of which: number of SMEs:	0	1
of which: number of entities in third countries (outside EU):	0	0
Targeted user audience: of reachable people	0	0
S&T publications (referenced publications only)	0	0
publications addressing general public (e.g. CD-ROMs, WEB sites)	0	0
publications addressing decision takers / public authorities / etc.	0	0
Visibility for the general public	NO	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development		**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
7	Fine grain reconfigurable block and supporting tools

CONTACT PERSON FOR THIS RESULT

Name	Dimitrios SOUDRIS
Position	Head of VLSI Systems Design Group
Organisation	Democritus University of Thrace
Address	12 V. Sofias 67100, Xanthi GREECE
Telephone	25410-79557
Fax	25410-79545
E-mail	dsoudris@ee.duth.gr
URL	www.duth.gr
Specific Result URL	http://vlsi.ee.duth.gr/amdrel

SUMMARY

The results are: (i) the circuit-level design of a fine-grain reconfigurable IP block and (ii) accompanying toolkit for supporting the design procedure. More specifically, the detailed design of the building blocks (CLB, switches, interconnections) including power optimization techniques, provide the fine-grain architecture. Using 0.18□Êm STM technology, a full-custom 8□~8 fine-grain IC was designed. To support alternative fine-grain reconfigurable architectures, i.e. design space exploration, function mapping, placement, routing, and reconfiguration bit-stream generation, a design environment based on public-domain and new tools as well as an appropriate user interface was developed.

SUBJECT DESCRIPTORS CODES
129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL 336 INTELLECTUAL PROPERTY 155 DESIGN, DESIGN ENGINEERING 579 SOFTWARE ENGINEERING, MIDDLEWARE, GROUPWARE 599 SYSTEMS DESIGN/THEORY 120 COMMUNICATION ENGINEERING/TECHNOLOGY

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential
Deliverable D26	Deliverable D26: Structure and organization of fine grain reconfigurable hardware	Confidential
Deliverable D27	D27: Fine grain reconfigurable hardware generator	Confidential
Deliverable D28	D28: Tool for technology mapping	Confidential
Deliverable D29	D29: Placement and routing tools	Confidential
Deliverable D30	D30: Configuration bitstream generator	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details (reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark							

applications						
Copyrights	√		journal and conference publications			
Secret know-how						
Other - please specify:						

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
30 Manufacture of office machinery and computers 32 Manufacture of radio, television and communication ☐ 72 Computer and related activities 73 Research and development 80 Education

CURRENT STAGE OF DEVELOPMENT

Current stage of development	Software code
Other:	

Quantified data about the result

Items (about the results)	**Actual current quantity**	**Estimated (or future) quantity**
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	√
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

Exploitation plans

CONFIDENTIAL

Description of the use and the dissemination of result(s), partner per partner

CONTRACT NUMBER:	IST-2001-34379
PARTNER's NAME:	INTRACOM S.A.

CONTACT PERSON(S):

Name	Konstantinos POTAMIANOS
Position/Title	Project Manager/Mr
Organisation	INTRACOM S.A.
Address	19,5 Km Markopoulo Ave., Peania, 190 02, Greece
Telephone	210-6671486
Fax	210-6671312
E-mail	cpot@intracom.gr

TITLE AND BRIEF DESCRIPTION OF MAIN RESULT(S)

Behavioural optimisation methodology and tool, i.e. i) the development of a systematic design methodology towards behavioral-level optimisation,and especially, the development of a novel methodology for energy- and performance-optimized design of dynamic memory allocators, ii) the development of a prototype design support software for addressing time-consuming task of dynamic memory management of the behavioral optimization approach. More specifically, the methodology is already finalized and the corresponding tool was completed by end of June 2004. Both methodology and tools target to wireless telecom applications.

TIMETABLE OF THE USE AND DISSEMINATION ACTIVITIES WITHIN THE NEXT 3 YEARS AFTER THE END OF THE PROJECT

Activity:	Investigation of ways integrating AMDREL methodologies within INTRACOM's wireless solutions
Timescale(month):	12
Brief description:	INTRACOM has already developed a series of wireless systems in order to provide voice, data and video services in rural, suburban and urban areas. AMDREL results will help upgrate our outdoor systems (both point-to-point and point-to-multipoint) as well as the development of new ones (e.g BFWA system operating at the 3,5GHz licensed and 5GHz unlicensed-exempt frequency bands)

FORESEEN COLLABORATIONS WITH OTHER ENTITIES

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement	√	**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement/Franchising	√	**INFO**	Information exchange	√
JV	Joint venture		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

Quantified data

Items	**Currently achieved quantity**	**Estimated future quantity**

Economic impacts (in EURO)	
number of licenses issued (within EU)	
numberof licenses issued (outside EU)	
Total value of licenses (in EURO)	
number of entrepreneurial actions (start-up company, joint ventures□)	
number of direct jobs created[c]	
number of direct jobs safeguarded[c]	
number of direct jobs lost	

Description of the use and the dissemination of result(s), partner per partner

CONTRACT NUMBER:	IST-2001-34379
PARTNER's NAME:	INTRACOM S.A.

CONTACT PERSON(S):

Name	Konstantinos POTAMIANOS
Position/Title	Project Manager/Mr
Organisation	INTRACOM S.A.
Address	19,5 Km Markopoulo Ave., Peania, 190 02, Greece
Telephone	210-6671486
Fax	210-6671312
E-mail	cpot@intracom.gr

TITLE AND BRIEF DESCRIPTION OF MAIN RESULT(S)

Optimised reusable soft intellectual properties for critical tasks of the target application domain. The result is an IP library of reusable VHDL-described components, which can perform critical tasks of systems in the targeted wireless communications domain. The main focus is on IPs for FFT, FIR filtering, taking into consideration plethora of design parameters will be delivered. These descriptions can be either directly mapped on the available reconfigurable hardware or used as input for the development of optimised lower level descriptions that can be directly on the available reconfigurable hardware.

TIMETABLE OF THE USE AND DISSEMINATION ACTIVITIES WITHIN THE NEXT 3 YEARS AFTER THE END OF THE PROJECT

Activity:	Investigation of ways integrating AMDREL methodologies within INTRACOM's wireless solutions
Timescale(month):	12
Brief description:	INTRACOM has already developed a series of wireless systems in order to provide voice, data and video services in rural, suburban and urban areas. AMDREL results will help upgrate our outdoor systems (both point-to-point and point-to-multipoint) as well as the development of new ones (e.g BFWA system operating at the 3,5GHz licensed and 5GHz unlicensed-exempt frequency bands).

FORESEEN COLLABORATIONS WITH OTHER ENTITIES

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement/Franchising	√	**INFO**	Information exchange	√
JV	Joint venture		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

Quantified data

Items	**Currently achieved quantity**	**Estimated future quantity**
Economic impacts (in EURO)		
number of licenses issued (within EU)		
numberof licenses issued (outside EU)		
Total value of licenses (in EURO)		
number of entrepreneurial actions (start-up company, joint ventures□)		
number of direct jobs created[c]		
number of direct jobs safeguarded[c]		
number of direct jobs lost		

Description of the use and the dissemination of result(s), partner per partner

CONTRACT NUMBER:	IST-2001-34379
PARTNER's NAME:	INTRACOM S.A.

CONTACT PERSON(S):

Name	Konstantinos POTAMIANOS
Position/Title	Project Manager/Mr
Organisation	INTRACOM S.A.
Address	19,5 Km Markopoulo Ave., Peania, 190 02, Greece
Telephone	210-6671486
Fax	210-6671312
E-mail	cpot@intracom.gr

TITLE AND BRIEF DESCRIPTION OF MAIN RESULT(S)

Fine grain reconfigurable block and sapporting tools. The results are: (i) the circuit-level design of a fine-grain reconfigurable IP block and (ii) accompanying toolkit for supporting the design procedure. More specifically, the detailed design of the building blocks (CLB, switches, interconnections) including power optimization techniques, provide the fine-grain architecture. Using 0.18□Êm STM technology, a full-custom 8□~8 fine-grain IC was designed. To support alternative fine-grain reconfigurable architectures, i.e. design space exploration, function mapping, placement, routing, and reconfiguration bit-stream generation, a design environment based on public-domain and new tools as well as an appropriate user interface was developed.

TIMETABLE OF THE USE AND DISSEMINATION ACTIVITIES WITHIN THE NEXT 3 YEARS AFTER THE END OF THE PROJECT

Activity:	Investigation of ways integrating AMDREL methodologies within INTRACOM's wireless solutions
Timescale(month):	12
Brief description:	INTRACOM has already developed a series of wireless systems in order to provide voice, data and video services in rural, suburban and urban areas. AMDREL results will help upgrate our outdoor systems (both point-to-point and point-to-multipoint) as well as the development of new ones (e.g BFWA system operating at the 3,5GHz licensed and 5GHz unlicensed-exempt frequency bands).

FORESEEN COLLABORATIONS WITH OTHER ENTITIES

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement/Franchising	√	**INFO**	Information exchange	√
JV	Joint venture		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

Quantified data

Items	**Currently achieved quantity**	**Estimated future quantity**
Economic impacts (in EURO)		
number of licenses issued (within EU)		
numberof licenses issued (outside EU)		
Total value of licenses (in EURO)		
number of entrepreneurial actions (start-up company, joint ventures□)		
number of direct jobs created[c]		
number of direct jobs safeguarded[c]		
number of direct jobs lost		

Overview of Exploitation Plans

RESULT TITLE / OWNER	COMMENT
Behavioural optimisation methodology and tool / INTRACOM S.A.	Exploitation plan included in eTIP
Optimised reusable soft intellectual properties for critical tasks of the target application domain / INTRACOM S.A.	Exploitation plan included in eTIP
Fine grain reconfigurable block and supporting tools / INTRACOM S.A.	Exploitation plan included in eTIP

I am the Co-ordinator of the above project, and confirm on behalf of the contracted Partners the information contained in this Technological Implementation Plan, and I authorise its public dissemination.

Signature: **Name:**

Date: **Organisation:**

close

TECHNOLOGICAL IMPLEMENTATION PLAN

Description of project

EC PROGRAMME:	**IST**
PROJECT TITLE:	Architectures and Methodologies for Dynamic Reconfigurable Logic
ACRONYM:	**AMDREL**
PROGRAMME TYPE:	5th FWP (Fifth Framework Programme)
CONTRACT NUMBER:	IST-2001-34379
PROJECT WEB SITE (if any):	http://www.vlsi.ee.duth.gr/amdrel
START DATE:	01 Mar 2002
END DATE:	28 Feb 2005
COORDINATOR DETAILS:	**Name:** Konstantinos POTAMIANOS **Organisation:** INTRACOM S.A. **Address:** 19,5 Km Markopoulo Ave., 190 02 Peania, Greece **Telephone:** +30-210-6671486 **E-mail:** cpot@intracom.gr

PARTNERS NAME:
Democritus University of Thrace, Dimitrios SOUDRIS **Interuniversitair Micro-Electronica Centrum Vzw,** Serge VERNALDE **ST Microelectronics Belgium (STMB),** Alun FOSTER

Commission Officer Name:	Markus Korn

Executive summary

Original research objectives
The main objective of the proposed project is to develop methodologies, tools and intellectual property blocks to be integrated in a mixed granularity dynamically reconfigurable SOC implementation platform for the efficient realization of wireless communications systems. The proposed methodology, tools, reusable intellectual property blocks and the mixed granularity reconfigurable implementation platform will be used for the development of systems from the wireless telecom domain including critical parts of a wireless LAN system. Thus the project targets potential system design users from wireless telecom domain, where a good balance between "flexibility" and implementation efficiency is needed during product's life-time.
Objectives: AMDREL's main objectives are: (a) Development of systematic methodologies for high level design tasks (such as behavioural optimisation wrt different implementation related factors and especially wrt power consumption, partitioning of targeted functionality to different types of reconfigurable hardware); (b) Development of reusable intellectual properties (including coarse granularity dynamically reconfigurable hardware blocks, low power fine-

granularity configurable logic blocks); (c) Instantiation of tools for implementation tasks; (d) Establishment of a dynamically reconfigurable SOC platform with mixed granularity components (fine and coarse grain); (e) Validation through demonstrators and; (f) Dissemination and use of results. Work description: AMDREL project will adopt an eight workpackages (WPs) workplan to achieve its objectives. The workpackages will: - explore target application domain to identify needs for behavioural optimisation and reconfigurability requirements; - explore reconfigurable platforms to identify requirements for high level implementation oriented optimisation; - refine the target mixed granularity reconfigurable architecture template; - select appropriate implementation technology (WP1); - develop methodology for domain and platform dependent behavioural optimisation; - develop prototype design support software for behavioural optimisation; - develop strategy for functionality partitioning between reconfigurable hardware blocks of different granularity; - develop prototype software for the core of the partitioning approach; - develop reusable soft intellectual properties for critical modules of the target application domain (WP2); - design coarse grain reconfigurable hardware blocks and supporting implementation approach (WP3); - design fine grain reconfigurable hardware blocks and supporting implementation tools (WP4); - design of interconnect network suitable for reconfigurable platforms and supporting tools (WP5); - develop demonstrators from the wireless LANs domain (WP6); - disseminate and use the project results through internet, conferences (WP7); - manage the project internally and towards the EC (WP8) Milestones: - Mixed granularity dynamically reconfigurable SOC architecture template by M9; - Systematic methodologies for behavioural optimisation and partitioning by M18; - High level tools and reusable IPs by M28; - Fine and coarse fain reconfigurable SOC components/interconnect network by M28; - Real life applications/demonstrators by M36; - Exploitation/dissemination concluding activities by M36.

Expected deliverables

D1 Behavioral optimization opportunities for wireless LAN systems, D2 Behavioral optimization requirements of reconfigurable platforms, D3 Requirements for interconnection networks in a dynamically reconfigurable context, D5 Refined mixed granularity dynamically reconfigurable target architecture template, D6 Selection of target implementation technology, D7 Existing functional level reconfigurable implementation platforms, D8 Critical functions from the target application domain suitable for implementation as reconfigurable blocks, D9 Survey of existing fine-grain reconfigurable hardware platforms, D10 Flexible and power efficient architectures for functional dynamically reconfigurable hardware blocks, D11 Network building blocks, D12 Dissemination and Use Plan (DUP) including web site by DUTH, D14 Power efficient configurable logic block, D15 Interconnect network simulation model and interconnect network instance generator, D16 Quality Assurance Plan, D18 Behavioral optimization methodology for wireless LAN systems realized on reconfigurable platforms, D19 Strategy for functionality partitioning between mixed granularity reconfigurable hardware blocks, D20 Functional reconfigurable modules, D21 Prototype source-to-source behavioral optimizer, D22 Prototype partitioning software, D23 Optimized reusable soft intellectual properties for critical tasks of the target application domain, D24 Definition and realization of efficient control mechanism, D25 Systematic methodology for implementation on the functional reconfigurable hardware blocks, D26 Structure and organization of fine grain reconfigurable hardware, D27 Fine grain reconfigurable hardware generator, D25 Tool for technology mapping, D29 Placement and routing tools, D30 Configuration bitstream generator, D31 Validation of interconnect network (implementation and performance test), D32 High level executable models of selected demonstrators, D33 Updated Dissemination and Use Plan, D36 Demonstrator based on processor for critical parts of the baseband function of wireless LANsystem, D37 Demonstrator based on multimedia application processor for wireless terminals, D38 Evaluation of AMDREL approach, D39 Updated Dissemination and Use Plan, D40 Technology Implementation Plan (TIP).

Project's actual outcome

-

Broad dissemination and use intentions for the expected outputs

-

Overview of all your main project results

No.	Self-descriptive title of the result	Category	Partner(s) owning the result

		A, B or C*	(s) (referring in particular to specific patents, copyrights, etc.) & involved in their further use
1	Network building blocks	B	Interuniversitair Micro-Electronica Centrum Vzw
2	Power efficient configurable logic block	B	Democritus University of Thrace
3	Interconnect network simulation model and interconnect network instance generator	B	Interuniversitair Micro-Electronica Centrum Vzw
4	Behavioural optimisation methodology and tool	B	INTRACOM S.A. Democritus University of Thrace
5	Optimised reusable soft intellectual properties for critical tasks of the target application domain	B	INTRACOM S.A. Democritus University of Thrace
6	Systematic methodology for implementation on the functional reconfigurable hardware blocks	B	ST Microelectronics Belgium (STMB)
7	Fine grain reconfigurable block and supporting tools	B	INTRACOM S.A. Democritus University of Thrace

* A: results usable outside the consortium / B: results usable within the consortium / C: non usable results

Quantified Data on the dissemination and use of the project results

Items about the dissemination and use of the project results (consolidated numbers)	Currently achieved quantity	Estimated future* quantity
Product innovations		
Process innovations		
New services (commercial)		
New services (public)		
New methods		
Scientific breakthrought		
Technical standards to which this project has contributed		
EU regulations/directives to which this project has contributed		
International regulations to which this project has contributed		
PhDs generated by the project		
Grantees/trainees including transnational exchange of personnel		

** "Future" means expectations within the next 3 years following the end of the project*

Comment on European Interest

Community added value and contribution to EU policies

European dimension of the problem

Contribution to developing S&T co-operation at international level. European added value

Contribution to policy design or implementation

Contribution to Community social objectives

Improving the quality of life in the Community:

Provision of appropriate incentives for monitoring and creating jobs in the

Community (including use and development of skills):
Supporting sustainable development, preserving and/ or enhancing the environment (including use/ conservation of resources):

Expected project impact (to be filled in by the project coordinator)

EU Policy Goals	I SCALE OF EXPECTED IMPACT OVER THE NEXT 10 YEARS -1 0 1 2 3	II other	
		Not applicable to project	Project Impacttoo difficult to estimate
1. Improved sustainable economic development and growth, competitiveness		√	√
2. Improved employment		√	√
3. Improved quality of life and health and safety		√	√
4. Improved education		√	√
5. Improved preservation and enhancement of the environment		√	√
6. Improved scientific and technological quality		√	√
7. Regulatory and legislative environment		√	√
8. Other		√	√

1. Economic development and growth, competitiveness	Scale of Expected Impacts over the next 10 years (2)	
	By Project End -1 0 1 2 3	After Project End -1 0 1 2 3
a) Increased Turnover for project participants - national markets		
b) Increased Turnover for project participants - international markets		
c) Increased Productivity for project participants		
d) Reduced costs for project participants		
e) Improved output quality/high technology content		

2. Employment	Scale of Expected Impacts over the next 10 years (2)	
	By Project End -1 0 1 2 3	After Project End -1 0 1 2 3
a) Safeguarding of jobs		
b) Net employment growth in projects participants staff		
c) Net employment growth in customer and supply chains		
d) Net employment growth in the European economy at		

large

3. Quality of Life and health and safety	Scale of Expected Impacts over the next 10 years (2)	
	By Project End -1 0 1 2 3	After Project End -1 0 1 2 3
a) Improved health care		
b) Improved food, nutrition		
c) Improved safety (incl. consumers and workers safety)		
d) Improved quality of life for the elderly and disabled		
e) Improved life expectancy		
f) Improved working conditions		
g) Improved child care		
h) Improved mobility of persons		

4. Improved education	Scale of Expected Impacts over the next 10 years (2)	
	By Project End -1 0 1 2 3	After Project End -1 0 1 2 3
a) Improved learning processes including lifelong learning		
b) Development of new university curricula		

5. Preservation and enhancement of the environment	Scale of Expected Impacts over the next 10 years (2)	
	By Project End -1 0 1 2 3	After Project End -1 0 1 2 3
a) Improved prevention of emissions		
b) Improved treatment of emissions		
c) Improved preservation of natural resources and cultural heritage		
d) Reduced energy consumption		

6. S&T quality	Scale of Expected Impacts over the next 10 years (2)	
	By Project End -1 0 1 2 3	After Project End -1 0 1 2 3
a) Production of new knowledge		
b) Safeguarding or development of expertise in a research area		
c) Acceleration of RTD, transfer or uptake		
d) Enhance skills of RTD staff		
e) Transfer expertise/know-how/technology		
f) Improved access to knowledge-based networks		
g) Identifying appropriate partners and expertise		
h) Develop international S&T co-operation		
i) Increased gender equality		

7. Regulatory and legislative environment	Scale of Expected Impacts over the next 10 years (2)	
	By Project End -1 0 1 2 3	After Project End -1 0 1 2 3
a) Contribution to EU policy formulation		
Contribution to EU policy implementation		

8. Other (please specify)	Scale of Expected Impacts over the next 10 years (2)	
	By Project End -1 0 1 2 3	After Project End -1 0 1 2 3

Description of Results

No.	Title
1	Network building blocks

CONTACT PERSON FOR THIS RESULT

Name	Serge Vernalde
Position	Technical Business Director
Organisation	Interuniversitair Micro-Elektronica Centrum vzw
Address	Kapeldreef 75 3001, Leuven Leuven
Telephone	+ 32-16-281-288
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URL	http://www.imec.be/
Specific Result URL	

SUMMARY

This result is an IP library of VHDL building blocks that can be used to build interconnect networks with different topologies on reconfigurable architectures. Such networks enable the dynamic creation and deletion of tasks on the reconfigurable hardware through their unified application interface. They form the basic components to explore and implement different interconnect networks depending on the requirements of the applications.

SUBJECT DESCRIPTORS CODES

120 COMMUNICATION ENGINEERING/TECHNOLOGY
129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL
155 DESIGN, DESIGN ENGINEERING
336 INTELLECTUAL PROPERTY
395 MICROELECTRONICS
599 SYSTEMS DESIGN/THEORY
600 SYSTEMS ENGINEERING

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU= Public CO= Confidential
Deliverable D11	Network building blocks	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate	Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate

	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for	√					√	EP 1372084 / US 2004-0049672
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights							
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
30 Manufacture of office machinery and computers 32 Manufacture of radio, television and communication ... 72 Computer and related activities 73 Research and development

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	Actual current quantity	Estimated (or future) quantity
Time to application / market (in months from the end of the research project)	0	0
Number of (public or private) entities potentially involved in the implementation of the result:	1	2
of which: number of SMEs:	0	0
of which: number of entities in third countries (outside EU):	1	2
Targeted user audience: of reachable people	5	5
S&T publications (referenced publications only)	7	3
publications addressing general public (e.g. CD-ROMs, WEB sites)	1	1
publications addressing decision takers / public authorities / etc.	1	0
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	

LIC	Licence agreement	√	**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
2	Power efficient configurable logic block

CONTACT PERSON FOR THIS RESULT

Name	
Position	
Organisation	
Address	,
Telephone	
Fax	
E-mail	
URL	
Specific Result URL	

SUMMARY

SUBJECT DESCRIPTORS CODES

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU= Public CO= Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate						Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen		Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick			
Patent applied for								
Patent granted								
Patent search carried out								
Registered design								
Trademark applications								
Copyrights								
Secret know-how								
Other - please specify:								

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	Actual current quantity	Estimated (or future) quantity
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development		FIN	Financial support	
LIC	Licence agreement		VC	Venture capital/spin-off funding	
MAN	Manufacturing agreement		PPP	Private-public partnership	
MKT	Marketing agreement		INFO	Information exchange/training	
JV	Establish a joint enterprise or partnership		CONS	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
3	Interconnect network simulation model and interconnect network instance generator

CONTACT PERSON FOR THIS RESULT

Name	Serge Vernalde
Position	Technical Business Director
Organisation	Interuniversitair Micro-Elektronica Centrum vzw
Address	Kapeldreef 75 B-3001, Leuven Leuven
Telephone	+ 32-16-281-288
Fax	+ 32-16-281-515
E-mail	Serge.Vernalde@imec.be
URL	http://www.imec.be/
Specific Result URL	

SUMMARY

This result provides the usage support to allow designers to build and integrate an interconnect network in several applications, using a library of network building blocks (D11). It consists of two major components. The first component comprises the simulation models of the network, which enables the modeling of the complete system that runs on the reconfigurable platforms. It allows to see the impact of different network technologies. The second component consists of the network instance generators, which will allow the designer to create a network according to the structure of the reconfigurable system he/she wants to develop.

SUBJECT DESCRIPTORS CODES
120 COMMUNICATION ENGINEERING/TECHNOLOGY 129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL 155 DESIGN, DESIGN ENGINEERING 395 MICROELECTRONICS 599 SYSTEMS DESIGN/THEORY 600 SYSTEMS ENGINEERING

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU= Public CO= Confidential
Deliverable D15	Interconnect network simulation model and interconnect network instance generator	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for	√					√	EP 1372084 / US 2004-0049672

Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights							
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
30 Manufacture of office machinery and computers 32 Manufacture of radio, television and communication ... 72 Computer and related activities 73 Research and development

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	**Actual current quantity**	**Estimated (or future) quantity**
Time to application / market (in months from the end of the research project)	0	0
Number of (public or private) entities potentially involved in the implementation of the result:	1	2
of which: number of SMEs:	0	0
of which: number of entities in third countries (outside EU):	1	2
Targeted user audience: of reachable people	5	5
S&T publications (referenced publications only)	7	3
publications addressing general public (e.g. CD-ROMs, WEB sites)	1	1
publications addressing decision takers / public authorities / etc.	1	0
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement	√	**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
	Establish a joint enterprise or				

JV	partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
4	Behavioural optimisation methodology and tool

CONTACT PERSON FOR THIS RESULT

Name	
Position	
Organisation	
Address	,
Telephone	
Fax	
E-mail	
URL	
Specific Result URL	

SUMMARY

SUBJECT DESCRIPTORS CODES

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU= Public CO= Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate						Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen		Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick			
Patent applied for								
Patent granted								
Patent search carried out								
Registered design								
Trademark applications								
Copyrights								
Secret know-how								
Other - please specify:								

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	Actual current quantity	Estimated (or future) quantity
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development		FIN	Financial support	
LIC	Licence agreement		VC	Venture capital/spin-off funding	
MAN	Manufacturing agreement		PPP	Private-public partnership	
MKT	Marketing agreement		INFO	Information exchange/training	
JV	Establish a joint enterprise or partnership		CONS	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
5	Optimised reusable soft intellectual properties for critical tasks of the target application domain

CONTACT PERSON FOR THIS RESULT

Name	
Position	
Organisation	
Address	,
Telephone	
Fax	
E-mail	
URL	
Specific Result URL	

SUMMARY

SUBJECT DESCRIPTORS CODES

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU= Public CO= Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights							
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents

2) Number of Internationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	Actual current quantity	Estimated (or future) quantity
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development		**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
6	Systematic methodology for implementation on the functional reconfigurable hardware blocks

CONTACT PERSON FOR THIS RESULT

Name	Alun FOSTER
Position	External projects manager
Organisation	ST Microelectronics Belgium (STMB)
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Telephone	
Fax	
E-mail	alun.foster@st.com
URL	
Specific Result URL	

SUMMARY

The methodology for implementing coarse-grained reconfigurable blocks begins from a high-level descritpion in SystemC. From the timed-functional description, a bridge is required to the implementation level. The methodology describes how to use an off-the-shelf design tool (from Target Compiler Technologies) to take timed functional models from SystemC and use a dedicated VLIW architecture as a physical instantiation of a coarse-grained reconfigurable block. Reconfiguration is achieved by providing the block with context-dependent machine code, controlled via externally applied switch options (the methodology also describes various methods for implementing this). The hardware definition of the reconfigurable engine is derived from an intermediate abstraction language "nML" which produces a dedicated compiler (C to machine code), a synthesisable HDL descritpion, and an instruction set simulator used to model the block at the cycle-accurate level in SystemC. The methodology permits iteration on the block architecture to be carried out very quickly, with immediate feedback on system performance through the integration into the complete SystemC environment. The use of a VLIW implementation does penalise memory requirements (programme store). However, this methodology is estimated to reduce the design time complex functions in multi-processor chains by as much as 50% compared to the "manual" methods presently available. The methodology is particularly applicable to, but not limited to, pipe-lined or daisy-chained computational tasks that must be implemented in an embedded sytem or integrated circuit.

SUBJECT DESCRIPTORS CODES
192 ELECTRONICS, ELECTRONIC ENGINEERING 155 DESIGN, DESIGN ENGINEERING 204 ENGINEERING, CONCURRENT ENGINEERING 395 MICROELECTRONICS

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU= Public CO= Confidential
IST-2001-34379-WP3-D24	Definition and Realization of an Efficient Control Mechanism	Confidential
IST-2001-34379-WP3-D25	Systematic Methodology for implementation of (coarse-grained) Reconfigurable Hardware Blocks	Public

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights							
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
32 Manufacture of radio, television and communication ... 72 Computer and related activities 73 Research and development

CURRENT STAGE OF DEVELOPMENT

Current stage of development	Guidelines, methodologies, technical drawings
Other:	Mthodology for internal use

Quantified data about the result

Items (about the results)	Actual current quantity	Estimated (or future) quantity
Time to application / market (in months from the end of the research project)	12	3
Number of (public or private) entities potentially involved in the implementation of the result:	0	1
of which: number of SMEs:	0	1
of which: number of entities in third countries (outside EU):	0	0
Targeted user audience: of reachable people	0	0
S&T publications (referenced publications only)	0	0
publications addressing general public (e.g. CD-ROMs, WEB sites)	0	0
publications addressing decision takers / public authorities / etc.	0	0
Visibility for the general public	NO	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development		**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
7	Fine grain reconfigurable block and supporting tools

CONTACT PERSON FOR THIS RESULT

Name	
Position	
Organisation	
Address	,
Telephone	
Fax	
E-mail	
URL	
Specific Result URL	

SUMMARY

SUBJECT DESCRIPTORS CODES

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU= Public CO= Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate						Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen		Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick			
Patent applied for								
Patent granted								
Patent search carried out								
Registered design								
Trademark applications								
Copyrights								
Secret know-how								
Other - please specify:								

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	Actual current quantity	Estimated (or future) quantity
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development		FIN	Financial support	
LIC	Licence agreement		VC	Venture capital/spin-off funding	
MAN	Manufacturing agreement		PPP	Private-public partnership	
MKT	Marketing agreement		INFO	Information exchange/training	
JV	Establish a joint enterprise or partnership		CONS	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

Exploitation plans

CONFIDENTIAL

Description of the use and the dissemination of result(s), partner per partner

CONTRACT NUMBER:	IST-2001-34379
PARTNER's NAME:	ST Microelectronics Belgium (STMB)

CONTACT PERSON(S):

Name	Alun FOSTER
Position/ Title	External Projects Manager/Mr
Organisation	ST Microelectronics Belgium (STMB)
Address	Excelsiorlaan 44-46 1930 Zaventem Belgium
Telephone	02/7181841
Fax	02/7181911
E-mail	alun.foster@st.com

TITLE AND BRIEF DESCRIPTION OF MAIN RESULT(S)

D25 - Systematic Methodology for implementation of (coarse-grained) Reconfigurable Hardware Blocks

TIMETABLE OF THE USE AND DISSEMINATION ACTIVITIES WITHIN THE NEXT 3 YEARS AFTER THE END OF THE PROJECT

Activity:	Signal processign system design
Timescale(month):	12
Brief description:	Design methodology enabling the implemention of processing functions as coarse-grained reconfigurable elements as sub-functions of a processing chain. Applicable to several communciations technologies, e.g. DSL, UWB, WLAN, Bluetooth. Can be used for evaluation and design of future IC components in our design centres.

FORESEEN COLLABORATIONS WITH OTHER ENTITIES

R&D	Further research or development		**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement/Franchising		**INFO**	Information exchange	
JV	Joint venture		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

Quantified data

Items	Currently achieved quantity	Estimated future quantity
Economic impacts (in EURO)		
number of licenses issued (within EU)		
numberof licenses issued (outside EU)		
Total value of licenses (in EURO)		
number of entrepreneurial actions (start-up company, joint ventures...)		
number of direct jobs created[c]		
number of direct jobs safeguarded[c]	0	6
number of direct jobs lost		

Overview of Exploitation Plans

RESULT TITLE / OWNER	COMMENT
Systematic methodology for implementation on the functional reconfigurable hardware blocks / ST Microelectronics Belgium (STMB)	Exploitation plan included in eTIP

close

TECHNOLOGICAL IMPLEMENTATION PLAN

Description of project

EC PROGRAMME:	**IST**
PROJECT TITLE:	Architectures and Methodologies for Dynamic Reconfigurable Logic
ACRONYM:	**AMDREL**
PROGRAMME TYPE:	5th FWP (Fifth Framework Programme)
CONTRACT NUMBER:	IST-2001-34379
PROJECT WEB SITE (if any):	http://www.vlsi.ee.duth.gr/amdrel
START DATE:	01 Mar 2002
END DATE:	28 Feb 2005
COORDINATOR DETAILS:	**Name:** Konstantinos POTAMIANOS **Organisation:** INTRACOM S.A. **Address:** 19,5 Km Markopoulo Ave., 190 02 Peania, Greece **Telephone:** +30-210-6671486 **E-mail:** cpot@intracom.gr

PARTNERS NAME:
Democritus University of Thrace, Dimitrios SOUDRIS **Interuniversitair Micro-Electronica Centrum Vzw,** Serge VERNALDE **ST Microelectronics Belgium (STMB),** Alun FOSTER

Commission Officer Name:	Markus Korn

Executive summary

Original research objectives
The main objective of the proposed project is to develop methodologies, tools and intellectual property blocks to be integrated in a mixed granularity dynamically reconfigurable SOC implementation platform for the efficient realization of wireless communications systems. The proposed methodology, tools, reusable intellectual property blocks and the mixed granularity reconfigurable implementation platform will be used for the development of systems from the wireless telecom domain including critical parts of a wireless LAN system. Thus the project targets potential system design users from wireless telecom domain, where a good balance between "flexibility" and implementation efficiency is needed during product's life-time.
Objectives: AMDREL's main objectives are: (a) Development of systematic methodologies for high level design tasks (such as behavioural optimisation wrt different implementation related factors and especially wrt power consumption, partitioning of targeted functionality to different types of reconfigurable hardware); (b) Development of reusable intellectual properties (including coarse granularity dynamically reconfigurable hardware blocks, low power fine-

granularity configurable logic blocks); (c) Instantiation of tools for implementation tasks; (d) Establishment of a dynamically reconfigurable SOC platform with mixed granularity components (fine and coarse grain); (e) Validation through demonstrators and; (f) Dissemination and use of results. Work description: AMDREL project will adopt an eight workpackages (WPs) workplan to achieve its objectives. The workpackages will: - explore target application domain to identify needs for behavioural optimisation and reconfigurability requirements; - explore reconfigurable platforms to identify requirements for high level implementation oriented optimisation; - refine the target mixed granularity reconfigurable architecture template; - select appropriate implementation technology (WP1); - develop methodology for domain and platform dependent behavioural optimisation; - develop prototype design support software for behavioural optimisation; - develop strategy for functionality partitioning between reconfigurable hardware blocks of different granularity; - develop prototype software for the core of the partitioning approach; - develop reusable soft intellectual properties for critical modules of the target application domain (WP2); - design coarse grain reconfigurable hardware blocks and supporting implementation approach (WP3); - design fine grain reconfigurable hardware blocks and supporting implementation tools (WP4); - design of interconnect network suitable for reconfigurable platforms and supporting tools (WP5); - develop demonstrators from the wireless LANs domain (WP6); - disseminate and use the project results through internet, conferences (WP7); - manage the project internally and towards the EC (WP8) Milestones: - Mixed granularity dynamically reconfigurable SOC architecture template by M9; - Systematic methodologies for behavioural optimisation and partitioning by M18; - High level tools and reusable IPs by M28; - Fine and coarse fain reconfigurable SOC components/interconnect network by M28; - Real life applications/demonstrators by M36; - Exploitation/dissemination concluding activities by M36.

Expected deliverables

D1 Behavioral optimization opportunities for wireless LAN systems, D2 Behavioral optimization requirements of reconfigurable platforms, D3 Requirements for interconnection networks in a dynamically reconfigurable context, D5 Refined mixed granularity dynamically reconfigurable target architecture template, D6 Selection of target implementation technology, D7 Existing functional level reconfigurable implementation platforms, D8 Critical functions from the target application domain suitable for implementation as reconfigurable blocks, D9 Survey of existing fine-grain reconfigurable hardware platforms, D10 Flexible and power efficient architectures for functional dynamically reconfigurable hardware blocks, D11 Network building blocks, D12 Dissemination and Use Plan (DUP) including web site by DUTH, D14 Power efficient configurable logic block, D15 Interconnect network simulation model and interconnect network instance generator, D16 Quality Assurance Plan, D18 Behavioral optimization methodology for wireless LAN systems realized on reconfigurable platforms, D19 Strategy for functionality partitioning between mixed granularity reconfigurable hardware blocks, D20 Functional reconfigurable modules, D21 Prototype source-to-source behavioral optimizer, D22 Prototype partitioning software, D23 Optimized reusable soft intellectual properties for critical tasks of the target application domain, D24 Definition and realization of efficient control mechanism, D25 Systematic methodology for implementation on the functional reconfigurable hardware blocks, D26 Structure and organization of fine grain reconfigurable hardware, D27 Fine grain reconfigurable hardware generator, D25 Tool for technology mapping, D29 Placement and routing tools, D30 Configuration bitstream generator, D31 Validation of interconnect network (implementation and performance test), D32 High level executable models of selected demonstrators, D33 Updated Dissemination and Use Plan, D36 Demonstrator based on processor for critical parts of the baseband function of wireless LANsystem, D37 Demonstrator based on multimedia application processor for wireless terminals, D38 Evaluation of AMDREL approach, D39 Updated Dissemination and Use Plan, D40 Technology Implementation Plan (TIP).

Project's actual outcome

-

Broad dissemination and use intentions for the expected outputs

-

Overview of all your main project results

No.	Self-descriptive title of the result	Category	Partner(s) owning the result

		A, B or C*	(s) (referring in particular to specific patents, copyrights, etc.) & involved in their further use
1	Network building blocks	B	Interuniversitair Micro-Electronica Centrum Vzw
2	Power efficient configurable logic block	B	Democritus University of Thrace
3	Interconnect network simulation model and interconnect network instance generator	B	Interuniversitair Micro-Electronica Centrum Vzw
4	Behavioural optimisation methodology and tool	B	INTRACOM S.A. Democritus University of Thrace
5	Optimised reusable soft intellectual properties for critical tasks of the target application domain	B	INTRACOM S.A. Democritus University of Thrace
6	Systematic methodology for implementation on the functional reconfigurable hardware blocks	B	ST Microelectronics Belgium (STMB)
7	Fine grain reconfigurable block and supporting tools	B	INTRACOM S.A. Democritus University of Thrace

*A: results usable outside the consortium / B: results usable within the consortium / C: non usable results

Quantified Data on the dissemination and use of the project results

Items about the dissemination and use of the project results (consolidated numbers)	Currently achieved quantity	Estimated future* quantity
Product innovations		
Process innovations		
New services (commercial)		
New services (public)		
New methods		
Scientific breakthrought		
Technical standards to which this project has contributed		
EU regulations/directives to which this project has contributed		
International regulations to which this project has contributed		
PhDs generated by the project		
Grantees/trainees including transnational exchange of personnel		

** "Future" means expectations within the next 3 years following the end of the project*

Comment on European Interest

Community added value and contribution to EU policies

European dimension of the problem

Contribution to developing S&T co-operation at international level. European added value

Contribution to policy design or implementation

Contribution to Community social objectives

Improving the quality of life in the Community:

Provision of appropriate incentives for monitoring and creating jobs in the

Community (including use and development of skills):
Supporting sustainable development, preserving and/or enhancing the environment (including use/conservation of resources):

Expected project impact (to be filled in by the project coordinator)

EU Policy Goals	**I SCALE OF EXPECTED IMPACT OVER THE NEXT 10 YEARS -1 0 1 2 3**	**II other**	
		Not applicable to project	**Project Impacttoo difficult to estimate**
1. Improved sustainable economic development and growth, competitiveness		√	√
2. Improved employment		√	√
3. Improved quality of life and health and safety		√	√
4. Improved education		√	√
5. Improved preservation and enhancement of the environment		√	√
6. Improved scientific and technological quality		√	√
7. Regulatory and legislative environment		√	√
8. Other		√	√

1. Economic development and growth, competitiveness	**Scale of Expected Impacts over the next 10 years (2)**	
	By Project End -1 0 1 2 3	**After Project End** -1 0 1 2 3
a) Increased Turnover for project participants - national markets		
b) Increased Turnover for project participants - international markets		
c) Increased Productivity for project participants		
d) Reduced costs for project participants		
e) Improved output quality/high technology content		

2. Employment	**Scale of Expected Impacts over the next 10 years (2)**	
	By Project End -1 0 1 2 3	**After Project End** -1 0 1 2 3
a) Safeguarding of jobs		
b) Net employment growth in projects participants staff		
c) Net employment growth in customer and supply chains		
d) Net employment growth in the European economy at		

large	

3. Quality of Life and health and safety	Scale of Expected Impacts over the next 10 years (2) By Project End -1 0 1 2 3	 After Project End -1 0 1 2 3
a) Improved health care		
b) Improved food, nutrition		
c) Improved safety (incl. consumers and workers safety)		
d) Improved quality of life for the elderly and disabled		
e) Improved life expectancy		
f) Improved working conditions		
g) Improved child care		
h) Improved mobility of persons		

4. Improved education	Scale of Expected Impacts over the next 10 years (2) By Project End -1 0 1 2 3	 After Project End -1 0 1 2 3
a) Improved learning processes including lifelong learning		
b) Development of new university curricula		

5. Preservation and enhancement of the environment	Scale of Expected Impacts over the next 10 years (2) By Project End -1 0 1 2 3	 After Project End -1 0 1 2 3
a) Improved prevention of emissions		
b) Improved treatment of emissions		
c) Improved preservation of natural resources and cultural heritage		
d) Reduced energy consumption		

6. S&T quality	Scale of Expected Impacts over the next 10 years (2) By Project End -1 0 1 2 3	 After Project End -1 0 1 2 3
a) Production of new knowledge		
b) Safeguarding or development of expertise in a research area		
c) Acceleration of RTD, transfer or uptake		
d) Enhance skills of RTD staff		
e) Transfer expertise/know-how/technology		
f) Improved access to knowledge-based networks		
g) Identifying appropriate partners and expertise		
h) Develop international S&T co-operation		
i) Increased gender equality		

7. Regulatory and legislative environment	Scale of Expected Impacts over the next 10 years (2) By Project End -1 0 1 2 3	 After Project End -1 0 1 2 3
a) Contribution to EU policy formulation		
Contribution to EU policy implementation		

8. Other (please specify)	Scale of Expected Impacts over the next 10 years (2) By Project End -1 0 1 2 3	 After Project End -1 0 1 2 3

Description of Results

No.	Title
1	Network building blocks

CONTACT PERSON FOR THIS RESULT

Name	Serge Vernalde
Position	Technical Business Director
Organisation	Interuniversitair Micro-Elektronica Centrum vzw
Address	Kapeldreef 75 3001, Leuven Leuven
Telephone	+32-16-281-288
Fax	+32-16-281-515
E-mail	Serge.Vernalde@imec.be
URL	http://www.imec.be/
Specific Result URL	

SUMMARY

This result is an IP library of VHDL building blocks that can be used to build interconnect networks with different topologies on reconfigurable architectures. Such networks enable the dynamic creation and deletion of tasks on the reconfigurable hardware through their unified application interface. They form the basic components to explore and implement different interconnect networks depending on the requirements of the applications.

SUBJECT DESCRIPTORS CODES
120 COMMUNICATION ENGINEERING/TECHNOLOGY 129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL 155 DESIGN, DESIGN ENGINEERING 336 INTELLECTUAL PROPERTY 395 MICROELECTRONICS 599 SYSTEMS DESIGN/THEORY 600 SYSTEMS ENGINEERING

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential
Deliverable D11	Network building blocks	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate	Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate

	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for	√					√	EP 1372084 / US 2004-0049672
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights							
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
30 Manufacture of office machinery and computers 32 Manufacture of radio, television and communication … 72 Computer and related activities 73 Research and development

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	**Actual current quantity**	**Estimated (or future) quantity**
Time to application / market (in months from the end of the research project)	0	0
Number of (public or private) entities potentially involved in the implementation of the result:	1	2
of which: number of SMEs:	0	0
of which: number of entities in third countries (outside EU):	1	2
Targeted user audience: of reachable people	5	5
S&T publications (referenced publications only)	7	3
publications addressing general public (e.g. CD-ROMs, WEB sites)	1	1
publications addressing decision takers / public authorities / etc.	1	0
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	

LIC	Licence agreement	√	**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
2	Power efficient configurable logic block

CONTACT PERSON FOR THIS RESULT

Name	
Position	
Organisation	
Address	,
Telephone	
Fax	
E-mail	
URL	
Specific Result URL	

SUMMARY

SUBJECT DESCRIPTORS CODES

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights							
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	Actual current quantity	Estimated (or future) quantity
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development		**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
3	Interconnect network simulation model and interconnect network instance generator

CONTACT PERSON FOR THIS RESULT

Name	Serge Vernalde
Position	Technical Business Director
Organisation	Interuniversitair Micro-Elektronica Centrum vzw
Address	Kapeldreef 75 B-3001, Leuven Leuven
Telephone	+32-16-281-288
Fax	+32-16-281-515
E-mail	Serge.Vernalde@imec.be
URL	http://www.imec.be/
Specific Result URL	

SUMMARY

This result provides the usage support to allow designers to build and integrate an interconnect network in several applications, using a library of network building blocks (D11). It consists of two major components. The first component comprises the simulation models of the network, which enables the modeling of the complete system that runs on the reconfigurable platforms. It allows to see the impact of different network technologies. The second component consists of the network instance generators, which will allow the designer to create a network according to the structure of the reconfigurable system he/she wants to develop.

SUBJECT DESCRIPTORS CODES
120 COMMUNICATION ENGINEERING/TECHNOLOGY 129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL 155 DESIGN, DESIGN ENGINEERING 395 MICROELECTRONICS 599 SYSTEMS DESIGN/THEORY 600 SYSTEMS ENGINEERING

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential
Deliverable D15	Interconnect network simulation model and interconnect network instance generator	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for	√					√	EP 1372084 / US 2004-0049672

Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights							
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
30 Manufacture of office machinery and computers 32 Manufacture of radio, television and communication … 72 Computer and related activities 73 Research and development

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	**Actual current quantity**	**Estimated (or future) quantity**
Time to application / market (in months from the end of the research project)	0	0
Number of (public or private) entities potentially involved in the implementation of the result:	1	2
of which: number of SMEs:	0	0
of which: number of entities in third countries (outside EU):	1	2
Targeted user audience: of reachable people	5	5
S&T publications (referenced publications only)	7	3
publications addressing general public (e.g. CD-ROMs, WEB sites)	1	1
publications addressing decision takers / public authorities / etc.	1	0
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement	√	**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
	Establish a joint enterprise or				

JV	partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
4	Behavioural optimisation methodology and tool

CONTACT PERSON FOR THIS RESULT

Name	
Position	
Organisation	
Address	,
Telephone	
Fax	
E-mail	
URL	
Specific Result URL	

SUMMARY

SUBJECT DESCRIPTORS CODES

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights							
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	Actual current quantity	Estimated (or future) quantity
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development		**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
5	Optimised reusable soft intellectual properties for critical tasks of the target application domain

CONTACT PERSON FOR THIS RESULT

Name	
Position	
Organisation	
Address	,
Telephone	
Fax	
E-mail	
URL	
Specific Result URL	

SUMMARY

SUBJECT DESCRIPTORS CODES

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights							
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents

2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	**Actual current quantity**	**Estimated (or future) quantity**
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development		**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
6	Systematic methodology for implementation on the functional reconfigurable hardware blocks

CONTACT PERSON FOR THIS RESULT

Name	
Position	
Organisation	
Address	,
Telephone	
Fax	
E-mail	
URL	
Specific Result URL	

SUMMARY

SUBJECT DESCRIPTORS CODES

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights							
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents

2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	**Actual current quantity**	**Estimated (or future) quantity**
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development		**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

No.	Title
7	Fine grain reconfigurable block and supporting tools

CONTACT PERSON FOR THIS RESULT

Name	
Position	
Organisation	
Address	,
Telephone	
Fax	
E-mail	
URL	
Specific Result URL	

SUMMARY

SUBJECT DESCRIPTORS CODES

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details (reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights							
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors

CURRENT STAGE OF DEVELOPMENT

Current stage of development	
Other:	

Quantified data about the result

Items (about the results)	Actual current quantity	Estimated (or future) quantity
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development		**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

Exploitation plans

CONFIDENTIAL

Description of the use and the dissemination of result(s), partner per partner

CONTRACT NUMBER:	IST-2001-34379
PARTNER's NAME:	Interuniversitair Micro-Electronica Centrum Vzw

CONTACT PERSON(S):

Name	Serge Vernalde
Position/Title	Technical Business Director/Mr
Organisation	Interuniversitair Micro-Electronica Centrum Vzw
Address	Kapeldreef 75, B-3001 Leuven
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TITLE AND BRIEF DESCRIPTION OF MAIN RESULT(S)

This result is an IP library of VHDL building blocks that can be used to build interconnect networks with different topologies on reconfigurable architectures. Such networks enable the dynamic creation and deletion of tasks on the reconfigurable hardware through their unified application interface. They form the basic components to explore and implement different interconnect networks depending on the requirements of the applications.

TIMETABLE OF THE USE AND DISSEMINATION ACTIVITIES WITHIN THE NEXT 3 YEARS AFTER THE END OF THE PROJECT

FORESEEN COLLABORATIONS WITH OTHER ENTITIES

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement	√	**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement/Franchising		**INFO**	Information exchange	
JV	Joint venture		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

Quantified data

Items	**Currently achieved quantity**	**Estimated future quantity**
Economic impacts (in EURO)	80000	160000
number of licenses issued (within EU)	0	0

numberof licenses issued (outside EU)	1	2
Total value of licenses (in EURO)	80000	160000
number of entrepreneurial actions (start-up company, joint ventures…)	0	0
number of direct jobs created[c]	5	2
number of direct jobs safeguarded[c]	3	2
number of direct jobs lost	0	0

Description of the use and the dissemination of result(s), partner per partner

CONTRACT NUMBER:	IST-2001-34379
PARTNER's NAME:	Interuniversitair Micro-Electronica Centrum Vzw

CONTACT PERSON(S):

Name	Serge Vernalde
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Telephone	+32-16-281-288
Fax	+32-16-281-515
E-mail	Serge.Vernalde@imec.be

TITLE AND BRIEF DESCRIPTION OF MAIN RESULT(S)

This result provides the usage support to allow designers to build and integrate an interconnect network in several applications, using a library of network building blocks (D11). It consists of two major components. The first component comprises the simulation models of the network, which enables the modeling of the complete system that runs on the reconfigurable platforms. It allows to see the impact of different network technologies. The second component consists of the network instance generators, which will allow the designer to create a network according to the structure of the reconfigurable system he/she wants to develop.

TIMETABLE OF THE USE AND DISSEMINATION ACTIVITIES WITHIN THE NEXT 3 YEARS AFTER THE END OF THE PROJECT

FORESEEN COLLABORATIONS WITH OTHER ENTITIES

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement	√	**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement/Franchising		**INFO**	Information exchange	
JV	Joint venture		**CONS**	Available for consultancy	
Other	(please specify)				
Details:					

Quantified data

Items	**Currently achieved quantity**	**Estimated future quantity**
Economic impacts (in EURO)	80000	160000
number of licenses issued (within EU)	0	0
numberof licenses issued (outside EU)	1	2
Total value of licenses (in EURO)	80000	160000
number of entrepreneurial actions (start-up company, joint ventures…)	0	0
number of direct jobs created[c]	5	2
number of direct jobs safeguarded[c]	3	2
number of direct jobs lost	0	0

Overview of Exploitation Plans

RESULT TITLE / OWNER	COMMENT
Network building blocks / Interuniversitair Micro-Electronica Centrum Vzw	Exploitation plan included in eTIP
Interconnect network simulation model and interconnect network instance generator / Interuniversitair Micro-Electronica Centrum Vzw	Exploitation plan included in eTIP

close

Description of Results

Title: Power efficient configurable logic block

CONTACT PERSON FOR THIS RESULT

Name	Dimitrios SOUDRIS
Position	Head of VLSI Systems Design Group
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E-mail	dsoudris@ee.duth.gr
URL	www.duth.gr
Specific Result URL	http://vlsi.ee.duth.gr/~dsoudris

SUMMARY

The result is the detailed architecture design of a power efficient configurable logic block (CLB), taking into consideration the constraints and limitations of the design supporting tools. Full-custom design using the chosen silicon technology of 0.18 um STM technology, exhaustive design exploration for selecting optimal design parameters, for instance number of look-up table inputs, in terms of power, area, and performance provided the appropriate results regarding with the design of configurable block. The low-energy CLB design of was the first critical step for implementing efficient low-energy fine-grain reconfigurable hardware.

SUBJECT DESCRIPTORS CODES

155 DESIGN, DESIGN ENGINEERING
129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL
336 INTELLECTUAL PROPERTY
395 MICROELECTRONICS
599 SYSTEMS DESIGN/THEORY

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential
Deliverable D14	Power efficient configurable logic block	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details(reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights	√			journal and conference publications			
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors

30 Manufacture of office machinery and computers
32 Manufacture of radio, television and communication ...
72 Computer and related activities
73 Research and development
80 Education

Quantified data about the result

Items (about the results)	Actual current quantity	Estimated (or future) quantity
Time to application / market (in months from the end of the research project)	12	24
Number of (public or private) entities potentially involved in the implementation of the result:	1	2
of which: number of SMEs:	1	1
of which: number of entities in third countries (outside EU):	0	1
Targeted user audience: of reachable people	4	9
S&T publications (referenced publications only)	7	2
publications addressing general public (e.g. CD-ROMs, WEB sites)	1	1
publications addressing decision takers / public authorities / etc.	0	0
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	√
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

Exploitation plans

CONFIDENTIAL

Description of the use and the dissemination of result(s), partner per partner

CONTRACT NUMBER:	IST-2001-34379
PARTNER's NAME:	Dimitrios SOUDRIS

CONTACT PERSON(S):

Name	Dimitrios SOUDRIS
Position/Title	Professor/Mr
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TITLE AND BRIEF DESCRIPTION OF MAIN RESULT(S)

Title: Power efficient configurable logic block Description: The result is the detailed architecture design of a power efficient configurable logic block (CLB), taking into consideration the constraints and limitations of the design supporting tools. Full-custom design using the chosen silicon technology of 0.18 um STM technology, exhaustive design exploration for selecting optimal design parameters, for instance number of look-up table inputs, in terms of power, area, and performance provided the appropriate results regarding with the design of configurable block. The low-energy CLB design of was the first critical step for implementing efficient low-energy fine-grain reconfigurable hardware.

TIMETABLE OF THE USE AND DISSEMINATION ACTIVITIES WITHIN THE NEXT 3 YEARS AFTER THE END OF THE PROJECT

Activity:	UnderGraduate & Graduate Courses
Timescale(month):	36
Brief description:	DUTH used the design of configurable logic block for teaching purposes, because it is an excellent case study for undergraduate students to understand the concepts of full-custom design of FPGAs, topic which is usually is not well-described in existing textbooks. More specifically, the undergraduate programme of DUTH includes two semester courses, VLSI Systems I & II. Concerning the graduate students, they may design their own configurable logic block using Europractice silicon technologies in context of the MSc and PhD semester courses “Design of Integrated Systems for Low Power” and “Integrated Systems of hardware and software”.

FORESEEN COLLABORATIONS WITH OTHER ENTITIES

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement/ Franchising		**INFO**	Information exchange	√
JV	Joint venture		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

QUANTIFIED DATA

Items	**Currently achieved quantity**	**Estimated future quantity**
Economic impacts (in EURO)		
number of licenses issued (within EU)		
numberof licenses issued (outside EU)		
Total value of licenses (in EURO)		

number of entrepreneurial actions (start-up company, joint ventures…)
number of direct jobs created[c]
number of direct jobs safeguarded[c]
number of direct jobs lost

Overview of Exploitation Plans

RESULT TITLE / OWNER	COMMENT
Power efficient configurable logic block / Democritus University of Thrace	Exploitation plan included in eTIP

Description of Results

Title: Behavioural optimisation methodology and tool

CONTACT PERSON FOR THIS RESULT

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E-mail	dsoudris@ee.duth.gr
URL	www.duth.gr
Specific Result URL	http://vlsi.ee.duth.gr/amdrel

SUMMARY

The results are: i) the development of a systematic design methodology towards behavioral-level optimisation,and especially, the development of a novel methodology for energy- and performance-optimized design of dynamic memory allocators and ii) the development of a prototype design support software for addressing time-consuming task of dynamic memory management of the behavioral optimization approach. More specifically, the methodology is already finalized and the corresponding tool was completed by end of June 2004. Both methodology and tools target to wireless telecom applications.

SUBJECT DESCRIPTORS CODES

155 DESIGN, DESIGN ENGINEERING
129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL
599 SYSTEMS DESIGN/THEORY
120 COMMUNICATION ENGINEERING/TECHNOLOGY
395 MICROELECTRONICS
600 SYSTEMS ENGINEERING

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential
Deliverable D18 and D21	The deliverable D18 addresses a systematic methodology for the implementation oriented behavioral optimization of high level descriptions of target systems. The implementation factors, on which the methodology focus, include data storage and transfers, namely dynamic data type refinement and dynamic memory management. The methodology consists of: a) the dynamic data type (DDT) refinement and b) the dynamic memory management (DMM) refinement. The deliverable D21 addresses the development of prototype source-to-source tools for the automation of the behavioral optimizations methodology. The main automation provided by our tool consist of the creation of highly customized dynamic memory managers with the use of DM Libraries that are part of the tool. The other automation consists of a tool to automate the transformation of C++ object oriented source code to procedural source code.	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details(reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							

Trademark applications						
Copyrights	√		journal and conference publications			
Secret know-how						
Other - please specify:						

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
30 Manufacture of office machinery and computers 32 Manufacture of radio, television and communication ... 72 Computer and related activities 73 Research and development

Quantified data about the result

Items (about the results)	**Actual current quantity**	**Estimated (or future) quantity**
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	√
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

Exploitation plans

CONFIDENTIAL

Description of the use and the dissemination of result(s), partner per partner

CONTRACT NUMBER:	IST-2001-34379
PARTNER's NAME:	Dimitrios SOUDRIS

CONTACT PERSON(S):

Name	Dimitrios SOUDRIS
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TITLE AND BRIEF DESCRIPTION OF MAIN RESULT(S)

Title: Behavioural optimisation methodology and tool Brief description: The results are: i) the development of a systematic design methodology towards behavioral-level optimisation,and especially, the development of a novel methodology for energy- and performance-optimized design of dynamic memory allocators and ii) the development of a prototype design support software for addressing time-consuming task of dynamic memory management of the behavioral optimization approach. More specifically, the methodology is already finalized and the corresponding tool was completed by end of June 2004. Both methodology and tools target to wireless telecom applications.

TIMETABLE OF THE USE AND DISSEMINATION ACTIVITIES WITHIN THE NEXT 3 YEARS AFTER THE END OF THE PROJECT

Activity:	UnderGraduate & Graduate Courses
Timescale(month):	36
Brief description:	DUTH will use the results for teaching purposes of graduate students in the course “Integrated Systems of Hardware and Software”, where 10 MSc and 4 Ph.D. students were enrolled, in average, each year. It is estimated that 15 MSc and 6 Ph.D. students will use the derived results during the preparation of their MSc and PhD theses for further research purposes.

FORESEEN COLLABORATIONS WITH OTHER ENTITIES

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement	√	**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement/ Franchising		**INFO**	Information exchange	√
JV	Joint venture		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

QUANTIFIED DATA

Items	Currently achieved quantity	Estimated future quantity
Economic impacts (in EURO)		
number of licenses issued (within EU)		
numberof licenses issued (outside EU)		
Total value of licenses (in EURO)		
number of entrepreneurial actions (start-up company, joint ventures…)		
number of direct jobs created[c]		
number of direct jobs safeguarded[c]		
number of direct jobs lost		

Overview of Exploitation Plans

RESULT TITLE / OWNER	COMMENT
Behavioural optimisation methodology and tool / Democritus University of Thrace	Exploitation plan included in eTIP

Description of Results

Title: Optimised reusable soft intellectual properties for critical tasks of the target application domain

CONTACT PERSON FOR THIS RESULT

Name	Dimitrios SOUDRIS
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E-mail	dsoudris@ee.duth.gr
URL	www.duth.gr
Specific Result URL	http://vlsi.ee.duth.gr/amdrel

SUMMARY

The result is an IP library of reusable VHDL-described components, which can perform critical tasks of systems in the targeted wireless communications domain. The main focus is on IPs for FFT, FIR filtering, taking into consideration plethora of design parameters will be delivered. These descriptions can be either directly mapped on the available reconfigurable hardware or used as input for the development of optimised lower level descriptions that can be directly on the available reconfigurable hardware.

SUBJECT DESCRIPTORS CODES

129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL
155 DESIGN, DESIGN ENGINEERING
336 INTELLECTUAL PROPERTY
395 MICROELECTRONICS
599 SYSTEMS DESIGN/THEORY

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential

Deliverable D23	Optimized reusable soft intellectual properties for critical tasks of the target application domain	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	**KNOWLEDGE:** **Tick a box and give the corresponding details(reference numbers, etc) if appropriate**					**Pre-existing know-how** **Tick a box and give the corresponding details(reference numbers, etc) if appropriate**	
	Current				**Foreseen**	**Tick**	**Details**
	Tick	**NoP[1)]**	**NoI[2)]**	**Details**	**Tick**		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights	√			journal and conference publications			
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors

30 Manufacture of office machinery and computers
32 Manufacture of radio, television and communication ...
72 Computer and related activities
73 Research and development
80 Education

Quantified data about the result

Items (about the results)	Actual current quantity	Estimated (or future) quantity
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement	√	**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	√
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

Exploitation plans

CONFIDENTIAL

Description of the use and the dissemination of result(s), partner per partner

CONTRACT NUMBER:	IST-2001-34379
PARTNER's NAME:	Dimitrios SOUDRIS

CONTACT PERSON(S):

Name	Dimitrios SOUDRIS
Position/Title	Professor/Mr
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Telephone	+30-25410-79557
Fax	+30-25410-79545
E-mail	dsoudris@ee.duth.gr

TITLE AND BRIEF DESCRIPTION OF MAIN RESULT(S)

Title: Optimised reusable soft intellectual properties for critical tasks of the target application domain Description: The result is an IP library of reusable VHDL-described components, which can perform critical tasks of systems in the targeted wireless communications domain. The main focus is on IPs for FFT, FIR filtering, taking into consideration plethora of design parameters will be delivered. These descriptions can be either directly mapped on the available reconfigurable hardware or used as input for the development of optimised lower level descriptions that can be directly on the available reconfigurable hardware.

TIMETABLE OF THE USE AND DISSEMINATION ACTIVITIES WITHIN THE NEXT 3

YEARS AFTER THE END OF THE PROJECT

Activity:	UnderGraduate & Graduate Courses
Timescale(month):	36
Brief description:	DUTH will use the results for teaching purposes of graduate students in the course “Low Power Design of Integrated Systems” and in the course “Designing Embedded Systems”, where the estimated number of enrolled student every academic year will be around 10 M.Sc. and 2 Ph.D. students. Also, the derived results will be used as case studies in Laboratory Exercises/Assignments in undergraduate lesson "VLSI Systems II" with an average of 35 enrolled students a year.

FORESEEN COLLABORATIONS WITH OTHER ENTITIES

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement	√	**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement/ Franchising		**INFO**	Information exchange	√
JV	Joint venture		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

QUANTIFIED DATA

Items	**Currently achieved quantity**	**Estimated future quantity**
Economic impacts (in EURO)		
number of licenses issued (within EU)		
numberof licenses issued (outside EU)		
Total value of licenses (in EURO)		
number of entrepreneurial actions (start-up company, joint ventures...)		
number of direct jobs created[c]		
number of direct jobs safeguarded[c]		

number of direct jobs lost	

Overview of Exploitation Plans

RESULT TITLE / OWNER	COMMENT
Optimised reusable soft intellectual properties for critical tasks of the target application domain / Democritus University of Thrace	Exploitation plan included in eTIP

Description of Results

Title: Fine grain reconfigurable block and supporting tools

CONTACT PERSON FOR THIS RESULT

Name	Dimitrios SOUDRIS
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Fax	+30-25410-79545
E-mail	dsoudris@ee.duth.gr
URL	www.duth.gr
Specific Result URL	http://vlsi.ee.duth.gr/amdrel

SUMMARY

The results are: (i) the circuit-level design of a fine-grain reconfigurable IP block and (ii) accompanying toolkit for supporting the design procedure. More specifically, the detailed design of the building blocks (CLB, switches, interconnections) including power optimization techniques, provide the fine-grain architecture. Using 0.18*f*Êm STM technology, a full-custom 8•~8 fine-grain IC was designed. To support alternative fine-grain reconfigurable architectures, i.e. design space exploration, function mapping, placement, routing, and reconfiguration bit-stream generation, a design environment based on public-domain and new tools as well as an appropriate user interface was developed.

SUBJECT DESCRIPTORS CODES

129 COMPUTER SCIENCE/ENGINEERING, NUMERICAL ANALYSIS, SYSTEMS, CONTROL
336 INTELLECTUAL PROPERTY
155 DESIGN, DESIGN ENGINEERING
579 SOFTWARE ENGINEERING, MIDDLEWARE, GROUPWARE
599 SYSTEMS DESIGN/THEORY

DOCUMENTATION AND INFORMATION ON THE RESULT

Documentation type	Details (Title, ref. number, general description, language)	Status: PU=Public CO=Confidential
Deliverable reports D26,D27, D28,D29,D30	D26: Structure and organization of fine grain reconfigurable hardware D27: Fine grain reconfigurable hardware generator D28: Tool for technology mapping D29: Placement and routing tools D30: Configuration bitstream generator	Confidential

INTELLECTUAL PROPERTY RIGHTS

Type of IPR	KNOWLEDGE: Tick a box and give the corresponding details(reference numbers, etc) if appropriate					Pre-existing know-how Tick a box and give the corresponding details(reference numbers, etc) if appropriate	
	Current				Foreseen	Tick	Details
	Tick	NoP[1)]	NoI[2)]	Details	Tick		
Patent applied for							
Patent granted							
Patent search carried out							
Registered design							
Trademark applications							
Copyrights	√			journal and conference publications			
Secret know-how							
Other - please specify:							

1) Number of **P**riority (national) applications/patents
2) Number of **I**nternationally extended applications/patents

MARKET APPLICATION SECTORS

Market application sectors
30 Manufacture of office machinery and computers 32 Manufacture of radio, television and communication ... 72 Computer and related activities 73 Research and development 80 Education

Quantified data about the result

Items (about the results)	**Actual current quantity**	**Estimated (or future) quantity**
Time to application / market (in months from the end of the research project)		
Number of (public or private) entities potentially involved in the implementation of the result:		
of which: number of SMEs:		
of which: number of entities in third countries (outside EU):		
Targeted user audience: of reachable people		
S&T publications (referenced publications only)		
publications addressing general public (e.g. CD-ROMs, WEB sites)		
publications addressing decision takers / public authorities / etc.		
Visibility for the general public	YES	

Further collaboration, dissemination and use of the result

COLLABORATIONS SOUGHT

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement		**INFO**	Information exchange/training	√
JV	Establish a joint enterprise or partnership		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

POTENTIAL OFFERED FOR FURTHER DISSEMINATION AND USE

PROFILE OF ADDITIONAL PARTNER(S) FOR FURTHER DISSEMINATION AND USE

Exploitation plans

CONFIDENTIAL

Description of the use and the dissemination of result(s), partner per partner

CONTRACT NUMBER:	IST-2001-34379
PARTNER's NAME:	Dimitrios SOUDRIS

CONTACT PERSON(S):

Name	Dimitrios SOUDRIS
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Fax	+30-25410-79545
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TITLE AND BRIEF DESCRIPTION OF MAIN RESULT(S)

Title: Fine grain reconfigurable block and supporting tools Description: The results are: (i) the circuit-level design of a fine-grain reconfigurable IP block and (ii) accompanying toolkit for supporting the design procedure. More specifically, the detailed design of the building blocks (CLB, switches, interconnections) including power optimization techniques, provide the fine-grain architecture. Using 0.18ƒÊm STM technology, a full-custom 8•~8 fine-grain IC was designed. To support alternative fine-grain reconfigurable architectures, i.e. design space exploration, function mapping, placement, routing, and reconfiguration bit-stream generation, a design environment based on public-domain and new tools as well as an appropriate user interface was developed.

TIMETABLE OF THE USE AND DISSEMINATION ACTIVITIES WITHIN THE NEXT 3 YEARS AFTER THE END OF THE PROJECT

Activity:	Training of Undergraduate and Graduate Students
Timescale(month):	36
Brief description:	Since May 2004 all tools can be accessed through AMDREL website. Also DUTH used the developed design flow for its students in the context of the 9th semester course VLSI Systems II (the average number of enrolled students is around 35) and in one Master's Thesis about reconfigurable architectures. DUTH will provide tutorial lectures in the Dept. of Electrical and Computer Engineering, University of Patras, Greece with the context MSc. Graduate studies "Integrated Systems of Hardware and Software". The average number of attendees was twenty (20) students. The lecture's topic is about "Architecture of Reconfigurable Hardware and Tools".

FORESEEN COLLABORATIONS WITH OTHER ENTITIES

R&D	Further research or development	√	**FIN**	Financial support	
LIC	Licence agreement		**VC**	Venture capital/spin-off funding	
MAN	Manufacturing agreement		**PPP**	Private-public partnership	
MKT	Marketing agreement/ Franchising		**INFO**	Information exchange	√
JV	Joint venture		**CONS**	Available for consultancy	√
Other	(please specify)				
Details:					

QUANTIFIED DATA

Items	**Currently achieved quantity**	**Estimated future quantity**
Economic impacts (in EURO)		
number of licenses issued (within EU)		
numberof licenses issued (outside EU)		

Total value of licenses (in EURO)
number of entrepreneurial actions (start-up company, joint ventures…)
number of direct jobs created[c]
number of direct jobs safeguarded[c]
number of direct jobs lost

Overview of Exploitation Plans

RESULT TITLE / OWNER	COMMENT
Fine grain reconfigurable block and supporting tools / Democritus University of Thrace	Exploitation plan included in eTIP